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10/601,617	06/23/2003	Louis A. Lippincott	42P17012	8912
8791 7590 08/06/2008 BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040				
EXAMINER				
NGUYEN, HAU H				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/601,617

Applicant(s)

LIPPINCOTT ET AL.

Examiner

HAU H. NGUYEN

Art Unit

2628

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 April 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 3-6 and 8-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3-6 and 8-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date 5/15/08
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. The response filed on 4/22/2008 has been fully considered in preparing for this Office Action.

Specification Objection

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The claimed subject matter in claims 6, 8-10 is not supported by the specification. In particular, the Specification does not provide any definition of “*a computer readable storage medium*”.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-6, 8-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Dao et al. (US. Patent No. 6,275,891) (“Dao”, hereinafter).

As per claim 1, Dao teaches *a method comprising:*

detecting an update to a register file accessible by a plurality of processing elements of a media signal processor when a processing element desires ownership of a selected hardware accelerator; (Dao teaches the media signal processor 206 comprises a plurality of processing elements DSP 0-DSP L-1 and a plurality of hardware accelerators ACCEL 0 – ACCEL M-1

(Fig. 2), wherein as shown in Fig. 4, processors can communicate by writing mailbox messages to other processors, see col. 6, lines 37-65, when the DSP 320 desires ownership to a selected hardware accelerator 318, it updates the registers in the mailbox to perform a function such as IDCT, the selected hardware accelerator 318 is thus granted the ownership to the DSP, see col. 8, lines 15-32);

enabling a hardware accelerator selected from a plurality of hardware accelerators according in response to at least one bit of a register within the register file that is set by a processing element when the processing element desires ownership of the selected hardware accelerator (Dao teaches the traffic master 204 handles processor to processor data transfers (col. 5, lines 6-14), and when a processor unit (e.g. a DSP) desires to access another processor unit (such as hardware accelerator) through the traffic master 204, the request processor unit should provide (besides address and data) an enable signal on one of the control lines, see col. 4, lines 32-53, and also writing to the mailbox of the selected hardware accelerator, as cited above in col. 8, lines 15-32); *and*

granting the processing element ownership over the selected hardware accelerator (the traffic master assert the “ready” signal to indicate that data is available, col. 4, lines 50-53, see also col. 8, lines 15-32 for an example of operation).

As per claim 3, Dao further teaches *enabling the selected hardware accelerator comprises:*

designating at least one register within the register file to receive control commands from the plurality of processing elements (as cited above, the processor units (e.g. DSP)

communicates with other processor units (such as hardware processor) by writing mailbox messages, col., lines 57-60); *and*

activating the selected hardware accelerator to perform a media processing function according to a control command detected within the register (col. 8, lines 15-32).

As per claim 4, Dao further teaches:

providing a selection unit coupled to the plurality of hardware accelerators (the traffic master 204, Fig. 2);

designating at least one register within the register file to receive control commands from the plurality of processing elements (asserting an enable signal to the control lines as cited above);

directing the selection unit to provide a processing element with access to a selected hardware accelerators (the traffic master 204 assert the ready signal to the requesting processor unit to indicate data is available, col. 4, lines 32-53); *and*

directing the selecting hardware accelerator to perform a media processing function according to a received control command (col. 8, lines 15-32).

As per claim 5, Dao also the step of *activating the selected hardware accelerator* comprises:

identifying a processing element having written the control command (determined by the traffic master 204 to identify which processor unit has asserted an enable signal, col. 4, lines 32-53);

determining, according to the control command, an input data stream for the selected hardware accelerator;

determining, according to the control command, an output data stream for the selected hardware accelerator (i.e., the hardware accelerator, based on the mailbox message written by the DSP, determines when to input data stream for processing, and when to output the data stream to the DSP, see col. 8, lines 15-32);

directing the selecting hardware accelerator to perform a media processing function according to a received control command (as cited above, col. 8, lines 15-32);

updating a control bit within a register of the register file to indicate whether data is available for one or more data dependent processing elements (as also cited above, the traffic master 204 asserts the ready signal to indicate data is available); and

requiring the one or more data dependent processing elements to wait to execute instructions until the data it needs to execute the instructions is available in one or more registers (Fig. 4, the MMU 406 resolves any conflicts (by delaying access attempts blocked by higher-priority accesses) and places conflict-free access patterns in the request queue 408, col. 6, lines 2-11).

Claim 6, which is similar in scope to claim 1, is thus rejected under the same rationale.

Claim 8, which is similar in scope to claim 3, is thus rejected under the same rationale.

Claim 9, which is similar in scope to claim 4, is thus rejected under the same rationale.

Claim 10, which is similar in scope to claim 5, is thus rejected under the same rationale.

As per claim 11, as shown in Fig. 2, Dao teaches a processor 206, comprising:

a plurality of processing elements (DSP0 – DSP L-1);

a plurality of hardware accelerators (ACCEL0-ACCEL m-1) coupled to a selection unit (traffic master 204); and

a register file coupled to the selection unit and the plurality of processing elements, the register file including a plurality of general purpose registers accessible by the plurality of hardware accelerators, the selection unit and the plurality of processing elements, at least one of the general purpose registers including at least one bit to allow a processing element to select a hardware accelerator in response to at least one bit of a register within the register file that is set by a processing element when the processing element desires ownership of the selected hardware accelerator; and

a control unit to direct the selection unit to activate the selected hardware accelerator to grant the processing element ownership over the selected hardware accelerator (addressed above, with reference to claims 1 and 4).

As per claim 12, Dao further teaches *wherein the plurality of processing elements comprise:*

an input processing element coupled to said register file, the input processing element to receive input data (i.e. processor unit that request for reading data); and

an output processing element coupled to the register file, the output processing element to transmit data (i.e. transmitting data to the hardware accelerator in the example on col. 8, lines 15-32).

Claim 13, which is similar in scope to claim 4, is thus rejected under the same rationale.

As per claim 14, Dao further teaches *wherein the control unit to identify a processing element having written a control command, and set a control bit within a register of the register file to indicate when data is available for the identified processing element from the selected hardware accelerator (determined by the traffic master 204 to identify which processor unit has*

asserted an enable signal, and assert the ready signal to the processor unit when data is available, col. 4, lines 32-53);

As per claim 15, Dao further teaches *a processing element to set a bit when the processing element desires selection of a hardware accelerator (as cited above) and set one more bits to identify one or more data dependent processing elements to prevent the identified processing elements from executing instructions until the one or more bits are reset* (col. 6, lines 60-65, i.e., the programmed write permission will prevent access of the DSP to the hardware accelerator in use in order to avoid conflict, see also col. 6, lines 2-10).

As per claim 16, as cited above, Dao teaches *the processing element to write a control command to a at least one register within the register file to direct a selected hardware accelerator to perform a media processing function according to the control command* (referring to claim 3) *and set a control bit to indicate the selected hardware accelerator is in use* (it is implied since the MMU control the request queue 408 free of conflict, col. 6, lines 2-10).

As per claim 17, Dao also teaches *a processing element to set one or more control bits within a register of the register file to identify one or more data dependent processing elements to stall the identified processing elements and prohibit execution of instructions until data required by the identified processing elements is available in one or more registers* (i.e. delaying access attempts blocked by higher priority accesses, col. 6, lines 2-10).

As per claims 18-20, Dao also teaches the hardware accelerators used in a multimedia system, therefore, including video processing hardware accelerators, audio processing hardware accelerators, and image processing hardware accelerators (col. 7, lines 63-65, and col. 1, lines 14-19).

As per claim 21, the scope of which is similar to claim 11, has been addressed above, further requires a plurality of media signal processors are coupled together, and a memory interface coupled to one or more of the media processors; and a random access memory coupled to the memory interface. This is also taught by Dao with reference to Fig. 3, memory interface 324, and memory 322. Dao further teaches the system are scalable (col. 8, lines 43-46), which means that plurality of media processors can be coupled together.

Claim 22, which is similar in scope to claim 3, is thus rejected under the same rationale.

Claim 23, which is similar in scope to claim 14, is thus rejected under the same rationale.

Claim 24, which is similar in scope to claim 15, is thus rejected under the same rationale.

Claim 25, which is similar in scope to claim 16, is thus rejected under the same rationale.

Claim 26, which is similar in scope to claim 17, is thus rejected under the same rationale.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al. (U.S. Patent No. 6,275,891) in view of McDonald et al. (U.S. Patent App. Pub. No. 2003/0028751).

As per claims 27, although Dao fails to explicitly teach or suggest the RAM is a SDRAM and/or DDRSDRAM, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to replace the random access memory as taught by Dao with

SDRAM or DDRSDRAM as indicated in McDonald et al. (Fig. 1, memory 16 can be an SDRAM, see page 2, par. 28) since SDRAM can be synchronized with the system bus, and thus, can be programmable for inputs as well as outputs.

Response to Arguments

Applicant's arguments filed 4/22/2008 have been fully considered but they are not persuasive. In response to Applicant's arguments that the cited reference fails to teach *detecting an update to a register file* and also fails to teach *granting the processing element ownership over the selected hardware accelerator*, the examiner respectfully disagrees. In response, as cited in the rejection, Dao teaches the traffic master 204, among other things, can enable inter-processor communication, which includes communication between DSP (processing element) and hardware accelerator, via mailbox messages (col. 5, lines 15-20). These mailbox messages are register files (col. 6, lines 30-35). As an example disclosed on column 8, lines 15-32, Dao teaches:

...The DSP 320 sends a message to the accelerator's mailbox to start the inverse discrete cosine transform of the decoded macroblock. The accelerator 318 performs the IDCT, writing pixel results to the MCU's memory (202C). Upon completion, the accelerator 318 sends a message to the MCU 104 requesting a transfer of the decoded video block to the video buffer.

Thus, the above excerpt shows that the DSP modify (update) the registers of the mailbox, when the DSP 320 desires ownership of the selected hardware accelerator 318 to perform the IDCT, granting the processing element (DSP 320) the ownership over the selected hardware accelerator 318 at the request of the processing element.

For at least the above reason, the cited reference Dao meets the requirement of the claims. Therefore, rejection is maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hau H Nguyen/

Examiner, Art Unit 2628

/Kee M Tung/

Supervisory Patent Examiner, Art Unit 2628